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PLANARIZATION METHOD FOR DEEP SUB MICRON SHALLOW TRENCH ISOLATION PROCESS

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

This invention relates to planarization of wafers using deep sub micron shallow trench isolation and more particularly to planarization methods using chemical mechanical polishing which avoids scratch marks on the planarized surface.

(2) DESCRIPTION OF THE RELATED ART

Shallow trench isolation is frequently used for isolation in integrated circuit wafers. With dense patterns in the active chip areas filling the trenches with dielectric results in uneven topology which must be planarized before subsequent processing steps are carried out. Chemical mechanical polishing is frequently used to accomplish this planarization but problems such as surface scratching must be overcome.

U.S. Pat. No. 6,180,525 to Morgan describes a method of minimizing repetitive chemical mechanical polishing scratch marks.

U.S. Pat. No. 5,728,621 to Zheng et al. describes a method of planarizing a high quality oxide used in shallow trench isolation.

U.S. Pat. No. 6,037,251 to Tu et al. describes a method for planarizing spin-on-glass used for intermetal insulation.

U.S. Pat. No. 6,270,353 to Andrews et al. describes a method for planarizing a structure such as a shallow trench isolation region.

U.S. Pat. No. 6,114,220 to Tsai describes a method of fabrication a shallow trench isolation including the formation of a trench in a substrate.

SUMMARY OF THE INVENTION

Shallow trench isolation is frequently used to isolate active areas on a insulated circuit wafers. When the trenches are filled with a dielectric the top surface of the dielectric can be very irregular and non planar, especially when large active areas are separated by isolation trenches. These irregular dielectric surfaces must be planarized prior to subsequent processing steps.

It is a principal objective of this invention to provide methods for planarizing wafers having shallow trench isolation with dielectric filling the trenches.

Shallow isolation trenches are formed in a semiconductor wafer, such as a silicon wafer, having devices formed therein. The isolation trenches isolate active areas of the chips in the wafer. The isolation trenches are then filled with a dielectric. The objective of this invention is achieved by forming a layer of resist material, such as photoresist, on the layer of dielectric used to fill the trenches. A polishing pad having a hardness of at least Shore "D" 52 is provided. The wafer is then planarized using this polishing pad and chemical mechanical polishing.

The planarization removes all of the resist and part of the dielectric, usually that part of the dielectric above the top surface of the wafer. If a pad oxide and a layer of silicon nitride are formed on the wafer before the isolation trenches are formed the planarization usually removes that part of the dielectric above the layer of silicon nitride.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A shows a cross section view of a semiconductor substrate having dielectric formed thereon.

Fig. 1B shows a cross section view of the dielectric showing a layer of pad oxide formed on the substrate and a layer of silicon nitride formed on the layer of pad oxide.

Fig. 2 shows a cross section view of the substrate of Fig. 1A after shallow isolation trenches have been formed.

Fig. 3 shows a cross section view of the substrate of Fig. 2 after a layer of dielectric has been deposited filling the isolation trenches.

Fig. 4 shows a cross section view of the substrate of Fig. 3 after a layer of resist has been formed on the layer of dielectric.

Fig. 5 shows a cross section view of the substrate of Fig. 4 after the substrate has been planarized.

Fig. 6 shows a schematic view of a chemical mechanical polishing apparatus having a polishing pad with a hardness of at least Shore "D" 52.

Fig. 7 shows a cross section view of a semiconductor substrate without a layer of pad oxide or a layer of silicon nitride after shallow isolation trenches have been formed and a layer of dielectric has been deposited filling the isolation trenches.

Fig. 8 shows a cross section view of the substrate of Fig. 7 after a layer of resist has been formed on the layer of dielectric.

Fig. 9 shows a cross section view of the substrate of Fig. 8 after the substrate has been planarized.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Refer now to Figs. 1A-9 for the following description of the preferred embodiments of the methods of this invention for planarizing substrates having shallow trench isolation. Fig. 1A shows a cross section view of a part of a wafer 40 comprising a substrate 10, such as a silicon substrate having devices formed therein, having a dielectric base 11 formed on the substrate 10. Any devices formed in the substrate are not shown in the Drawings since they are not critical to the methods of this invention. As shown in Fig. 1B the dielectric base 11 is usually, but not necessarily, a layer of pad oxide 12 formed on the substrate 10 and a layer of silicon nitride 14 formed on the layer of pad oxide. The dielectric base 11 could also be a single dielectric material.

As shown in Fig. 2, trench openings are formed in the dielectric base 11 and trenches are formed in the substrate 10. The trenches segment the substrate 10 into smaller active areas 17, larger active areas 19, and trenches. Next as shown in Fig. 3, a layer of trench dielectric 18 is deposited on the substrate filling the trenches with trench dielectric 18. The trench dielectric 18 is a relatively dense dielectric such as silicon dioxide deposited using high density plasma chemical vapor

deposition. As shown in Fig. 3, the trench dielectric 18 forms a very irregular top surface due to the trenches, the smaller active areas 17, and the larger active areas 19. The parts of the top surface of the layer of trench dielectric 18 over the larger active areas 19 will be higher than the parts over the smaller active areas 17 and over the trenches.

As shown in Fig. 4 a layer of resist 20, such as photoresist, is formed on the layer of trench dielectric 18. The resist 20 can be deposited using a method such as spinning liquid resist on the substrate and forms a planar top surface even though it is formed on a layer of trench dielectric 18 having an irregular top surface. The resist is then cured, usually by baking the resist. Next the wafer 40 is planarized by removing all of the resist 20 and a part of the trench dielectric 18. This planarization is accomplished using a hard polishing pad and chemical mechanical polishing. Fig. 5 shows the wafer 40 after the planarization has been completed showing trench dielectric 18 remaining in the trenches and a wafer 40 having a planar top surface. That part of the trench dielectric 18 above the top surface of the base dielectric 11 is usually removed.

Fig. 6 shows a schematic view of a chemical mechanical polishing apparatus. The apparatus comprises a hard polishing pad 32 on a rotating base 30. The rotating base is attached to a shaft 34 which rotates the base 30. The wafer to be planarized 40 is attached to a wafer holder 36. The wafer holder 36 is attached to a shaft 38 which both positions the wafer 40 relative to the polishing pad 32 and rotates the wafer 40 during the polishing.

One of the key features of this invention is that the polishing pad 32 is very hard having a hardness of at least Shore "D" 52. This hard polishing pad planarizes the wafer without leaving scratch marks on the remaining trench dielectric 18, any base dielectric 11 on the surface of the substrate 10, or the surface of the substrate 10 if there is no base dielectric 11 used on the substrate 10. No etching other than the chemical mechanical polishing is required for the planarization of the wafer.

This invention can also be used if there is no base dielectric 11 formed on the substrate 10. Fig. 7 shows a cross section of a wafer 40 with no base dielectric formed on the substrate 10, trenches formed in the substrate 10, and a layer of trench dielectric 18 formed on the substrate 10 wherein the trench dielectric 18 fills the trenches. As in the preceding embodiment the trenches segment the

substrate 10 into smaller active areas 17 and larger active areas 19. As in the preceding embodiment, the trench dielectric 18 is a relatively dense dielectric such as silicon dioxide deposited using high density plasma chemical vapor deposition. As shown in Fig. 7, the trench dielectric 18 forms a very irregular top surface due to the trenches, the smaller active areas 17, and the larger active areas 19. The parts of the top surface of the layer of trench dielectric 18 over the larger active areas 19 will be higher than the parts of the trench dielectric 18 over the smaller active areas 17 and over the trenches.

As shown in Fig. 8 a layer of resist 20, such as photoresist, is formed on the layer of trench dielectric 18. The resist 20 can be deposited using a method such as spinning liquid resist on the substrate and forms a planar top surface even though it is formed on a layer of trench dielectric 18 having an irregular top surface. The resist is then cured, usually by baking the resist.

Next the wafer 40 is planarized by removing all of the resist 20 and a part of the trench dielectric 18. This planarization is accomplished using a hard polishing pad and chemical mechanical polishing. Fig. 9 shows the wafer 40 after the planarization has been completed showing trench dielectric 18 remaining in the trenches and a wafer 40

having a planar top surface. Usually that part of the trench dielectric 18 above the top surface of the substrate 10 is removed. As in the preceding embodiment the planarization is accomplished using chemical mechanical polishing, a hard polishing pad, and chemical mechanical polishing apparatus, as shown in Fig. 6 and described in the preceding embodiment.

In this embodiment, as in the preceding embodiment, a key to the invention is that the polishing pad 32, see Fig. 6, is very hard having a hardness of at least Shore "D" 52. This hard polishing pad planarizes the wafer without leaving scratch marks on the remaining trench dielectric 18 or on the surface of the substrate 10. No etching other than the chemical mechanical polishing is required for the planarization of the wafer.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is: